High-Speed, 100+ W RF Switches Using GaAs MMICs

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***Abstract*—We have developed a low-loss, inductive gate bias network structure which allows very high stacking level of FET devices for high-power rf switching applications. We describe the design, implementation, and performance of *S*- and *C*-band SPDT switches based on this structure, using multiple GaAs MMIC chips integrated into a suspended-substrate hybrid circuit. At *S*-band, we demonstrated switch rise-fall times of less than 40 ns and an rf power handling capability of 300 W CW. This input signal level could be maintained during the switch state transitions ('hot-switching'), while being switched between the two output ports at rates up to 500 KHz.**

I. Introduction

CURRENT solid-state high-power rf switches are typically constructed using silicon p-i-n diodes. These low-cost devices can be made to have very high power handling capability and low distortion, at the expense of switching speed. Though silicon p-i-n-diodes are well-suited for controlling pulsed-rf signals, it is very difficult to adapt them to applications which, for instance, require both high CW power handling and high switching rates. In fact, because of the rf energy dissipated in the diode during its relatively long switching transient, the 'hot-switching' power rating of p-i-n switches (i.e., the maximum rf power level applied during the switch state transition) is typically much lower than the steady-state value, even at low switching rates. Also, the high-voltage driver circuits required to get optimum switching characteristics out of silicon p-i-n diodes tend to be complex, bulky, and expensive.

On the other hand, GaAs MESFETs provide intrinsically short switching times with simple, low-voltage driver circuits, and are used extensively for low-power switching applications. Using these devices, switch power handling capabilities up to 20 W and 27 W have been demonstrated in single-chip [1]–[3] and hybrid MMIC implementations [4], respectively. These circuits overcome the power handling limitation associated with the voltage breakdown characteristics of MESFETs by using an impedance transformation [1], by using multiple-gate devices [2], [3], and by stacking devices in series [4]. This paper describes how we used this latter approach to implement high-speed SPDT switch units with a hot-switching CW power handling capability of 100 + watts and approximately 10% operating bandwidth at *S*- and *C*-band frequencies.

Several critical problems had to be solved in order to implement a MESFET switch that could operate at such high power levels. The first was that the resistive gate bias networks used in previous designs would lead either to excessively high rf power dissipation, or very poor switching speed performance. Another was to find a way of minimizing the parasitic capacitance and inductance of the stacked MESFET structure to allow sufficiently high operating frequency and bandwidth. Also, we had to devise a mechanical design that would provide the necessary thermal dissipation and allow for practical assembly procedure and relatively easy replacement of the individual hybrid switching elements that make up the SPDT switch units. Finally, it was necessary to develop a suitable screening test procedure of these hybrid elements so that flaws could be detected and fixed before high-power testing of the fully-assembled unit. This was important because we had only limited access to high-power testing equipment and, at these power levels, failure of one element could lead to the destruction of most of the other elements, resulting in costly repairs.

II. FET and Gate Bias Network Considerations

For optimum power handling, bandwidth and switching performance, the FET periphery (total gate width) should be chosen so that the saturation current (Idss) of the FET is approximately equal to the peak rf current that passes through it in its ON state. As described in [4], the power handling capability of MESFET switches can be greatly enhanced by simultaneously increasing their periphery and by stacking *N*-devices in series. If the rf voltage swing is evenly divided within a stack of *N* FETs connected in series, the maximum power P_{max} that can be handled is given by [4]:

$$P_{max} = \frac{N^2 (V_B - V_P)^2}{2Z_o} \quad (1)$$

Where Z_o is the characteristic impedance of the system, V_B and V_P are the gate-drain (or gate-source) breakdown and the pinchoff voltage of the FET, respectively. A

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stacking level of $N = 15$ was deemed necessary to achieve the power handling objective of this program with the voltage breakdown characteristics of FETs currently available from GaAs foundries. Ideally, the FET's power handling capability per unit gate periphery is independent of stacking level, as the size of each FET in the stack increases proportionally to N. Thus, for devices with power-handling density of 2.2 W/mm gate periphery, a total of 227 mm of FET gate periphery per stack is needed to handle 500 W of rf power.

Typically, microwave MESFET switches are biased through a large-valued resistor connected in series with the gate, to allow the total rf voltage swing across the device to be equally shared between the gate-source and gate-drain electrode pairs. The loss due to the rf voltage swing across the gate bias resistor is usually negligible for single-FET switches. However, in an N-FET stack with bias resistors of value R in series with each FET gate, it can be shown that the power loss P_{dis}, normalized to the rf power P is given by

$$\frac{P_{\text{dis}}}{P} = \frac{Z_o(4N^2 - 1)}{12NR}. \tag{2}$$

or, using (9) in [4], and scaling FET periphery by N:

$$\frac{P_{\text{dis}}}{P} = \frac{Z_o C_{ge}(4N^2 - 1)}{12\tau}. \tag{3}$$

Where τ is the switching time, and C_{ge} is the effective gate junction capacitance for a single FET switch with optimum periphery for power handling. Equations (2) and (3) assume that R is large enough to allow even distribution of the rf voltage across the electrodes of all the FETs in the stack [4]. Equation (3) shows that, for a given switching time, the intrinsic rf loss associated with gate bias network increases proportionally to the power handling capability of the FET stack. Assuming $N = 15$ and typical values of $C_{ge} = 1.5$ pF, $Z_o = 50\ \Omega$ then, with a switching time goal of less than 50 ns, the gate network loss figure would be more than 0.5 dB per switch stack. For a multiple-section switch, with additional ohmic losses and the finite 'on' and 'off' resistances of the FET drain-source channel, such high loss from the gate bias network alone was unacceptable.

To overcome this problem, we used a low loss, inductive bias network [5]. The topology of the basic version of this network is shown in Fig. 1. In this design, the control voltage Vg is transmitted to each of the FET gates in the stack via a chain of inductors and a series resistor. The high reactance of these inductors allows the total rf voltage swing to be evenly divided between the gate-source and gate-drain terminals of the FETs. Hence, as for the typical resistive network discussed above, the value L of the individual inductors must be chosen so that the magnitude of their reactance is significantly higher than that of the off-state (pinched-off) gate capacitance (C_{gp}) at the minimum operating frequency f. But, if L is too large, the inductors become difficult to fabricate and the switching time becomes excessive. A satisfactory compromise is to use inductors with a reactance magnitude about seven times larger than that of Cgp, namely:

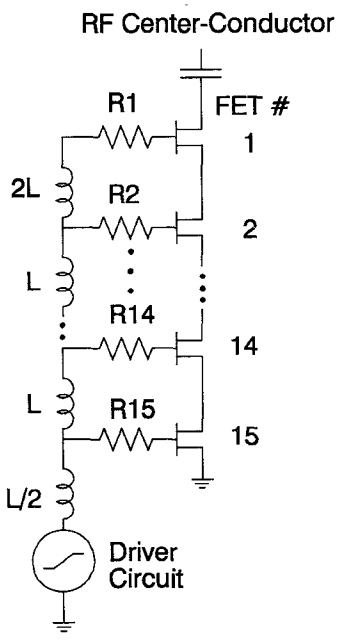

Fig. 1. Simplified schematic of the inductive gate bias network for the high-power stacked FET structure.

$$L = \frac{7}{C_{gp}(2\pi f)^2}. \tag{4}$$

In order for L to be as low as this, the inductor at the top of the chain has to have a value $2L$. This is because nearly all the rf current through the inductor chain flows from the top drain terminal, through the gate junctions of the upper FETs in the stack. Setting the top inductor value to $2L$ equalizes the rf current through the gates of the top two FETs, and limits the imbalance in the gate-source and gate-drain rf voltage swing for the top FET. The inductor at the bottom of the chain has a value of $L/2$, as it sees only half the rf voltage swing of the other inductors.

The series gate resistors ($R1$ through Rn in Fig. 1) serve two functions. One is to dampen the gate voltage 'ringing' that would otherwise occur in the inductive bias network during the switching transients. The other function is to equalize the switching times of the FETs in the stack: the values of the resistors decrease monotonically from the bottom to the top of the stack. The variable RC time constants thus obtained compensate for the delay of the switching signal as it propagates up the inductor chain.

For reasons described in Section III, a capacitor had to be placed between the rf line and the top of the FET stack, blocking any dc current through this path. In the steady pinched-off state of the stack, the finite 'off' state resistance of drain-source channels prevented the small dc gate leakage currents from driving the FETs out of the pinch-off. For S-band switch, the upper value of this 'off' state resistance was limited by large (≈ 10 kΩ) resistors integrated in parallel with the drain-source electrodes of each

FET. It was essential that the FETs in the stack be pinched-off sequentially from top to bottom during the switch-off transients. Otherwise the gate junctions of the upper FETs have to be charged through the large drain-source channel resistance of the pinched-off FETs below them, and the overall switching time for the stack can increase dramatically.

If the losses in the inductors are negligible then, for optimum damping, the value of smallest series gate resistor ($R1$ in Fig. 1) should be approximately equal to the magnitude of the reactance of the FET gate capacitance at the resonant frequency of the bias circuit. For this purpose, the bias circuit can be viewed as a low-pass, lumped element transmission line structure formed by the bias inductors and the FET junction capacitances. Assuming that the resonance occurs at the quarter-wavelength frequency of this structure, then:

$$R1 \approx \frac{4NZ_b}{2\pi}$$

$$Z_b = \sqrt{\frac{L}{\overline{C}_g}} \tag{5}$$

Where $\overline{C}g$ is the average gate capacitance over the control voltage excursion. In practice, the finite loss of the bias inductors allows $R1$ to be made smaller than the (5) value.

Using the same transmission line analogy, the time needed to switch all the FETs off (i.e., the rf rise-time in a shunt switch configuration) can be calculated as being approximately equal to the reflection delay of the line, namely:

$$\tau_{\text{off}} \approx 2N\sqrt{L\overline{C}_g} \tag{6}$$

The value of the lower series gate resistor ($R15$ in Fig. 1) should be chosen so that the R_NC_g time constant is at least equal to this delay:

$$R_N \geq \frac{\tau_{\text{off}}}{\overline{C}_g} = 2NZ_b. \tag{7}$$

We used a time-domain analysis program (PSPICE) to determine the optimum taper (linear or piece-wise linear) for the intermediate resistors $R2$ through $R14$, so as to obtain the required sequential switching of all the FETs in the stack, as discussed earlier. Our simulations were based on a slightly modified version of the GaAs FET model developed by Statz *et al.* [6]. The modifications consisted of adding fixed gate-source and gate-drain capacitors, and a drain-source resistor between the nodes of the intrinsic FET model to get more accurate representation of the device's capacitance distribution and loss in the pinched-off state.

Fig. 2 shows simulation results for a 15 FET shunt stack, with the Fig. 1 gate bias network, during the FET turn-off transient. This simulation corresponds to hot-switching conditions in a SPDT switch, with a total of 224 V peak rf swing across the stack in its 'off' state (500 W in a 50 Ω system). It can be seen that even during the transients, the rf voltage swing is fairly evenly distributed across the drain-source electrodes of most of the FETs in the stack. The top two FETs in the stack have lower steady-state rf voltage swings across them because their gate electrodes carry most of the rf current through the inductive bias network, as discussed earlier. The potential reliability problems associated with the slight increase in rf voltage swing seen by some devices in the stack during the transients can be eliminated through make-before-break timing of the switch control signals, as described in Section IV.

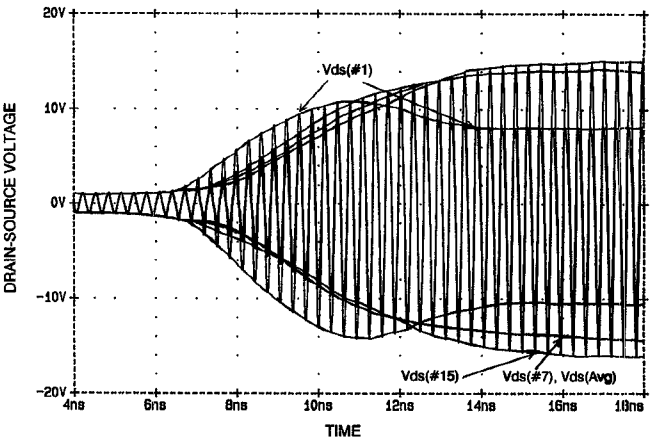

Fig. 2. Simulated rf voltage swing across the drain-source electrodes for the FET #1, 7, and 15 in the Fig. 1 structure during the FET turn-off transients. The average voltage swing across each FET in the stack is also plotted for reference. The gate drive waveform is a voltage step starting from 0 V at 4 ns to −11.6 V at 10 ns.

III. RF Circuit Design

The topology of the *S*-band SPDT rf switch circuits is shown in Fig. 3. The characteristic impedances of the Z1 and Z2 lines are 50 and 70 Ω, respectively. The Z2 lines compensate for the parasitic capacitances associated with the shunt MMIC switches. Their characteristic impedance was chosen so that their lengths would be comparable to the physical width of the MMIC chips and gate bias circuits in the shunt switch circuits (labeled W1 and W2 in Fig. 3). The stack FET MMICs in the W1 and W2 switch circuits had a peripheries of 3.8 and 2.9 mm/FET, respectively: as the W2 circuits carry little rf current, their size was reduced to minimize insertion loss. A similar circuit topology was used for the *C*-band switch unit.

The capacitors in series with the stack-FET MMICs tune-out their parasitic inductance in the operating band so as to maximize the isolation of the switch. However, these capacitors also act as dc blocks which limit the charge transfer between the gate junctions of the FETs and the rf line. This reduces the 'video leakage', but it also complicates the gate bias network design, as mentioned in section II. The lines labeled Z3 in Fig. 3 have a characteristic impedance of 45 Ω to increase the bandwidth of the circuit by lowering the in-band SWR associated with the T-junction between the two switch arms.

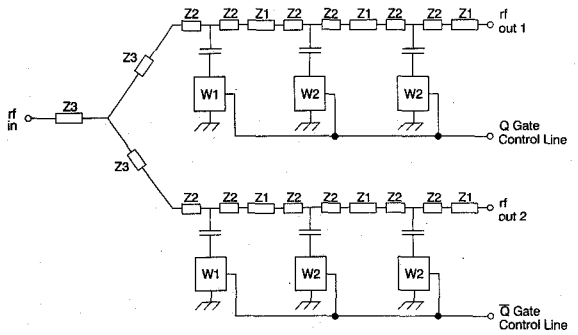

Fig. 3. Circuit topology of the high-power *S*-band SPDT switch unit. The W1 and W2 blocks are the stack-FET switch circuits detailed in Fig. 1. Each stack, together with its associated capacitor and transmission lines Z1 and Z2, was implemented as a separate, replaceable element as shown in Fig. 6.

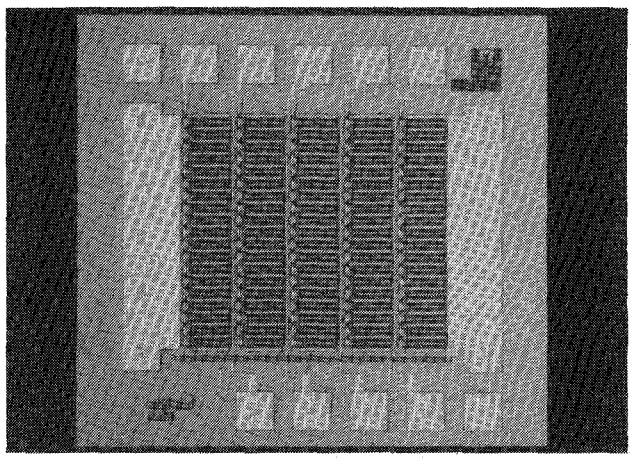

Fig. 4. Picture of the stack-FET MMIC chip used in the *S*-band switch elements. Chip size is 1.05 × 1.05 mm^2.

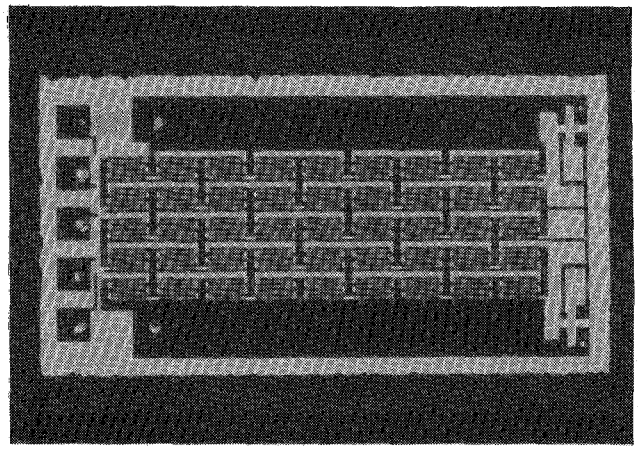

Fig. 5. Picture of the stack-FET MMIC chip used in the *C*-band switch element. Chip size is 0.82 × 1.63 mm^2.

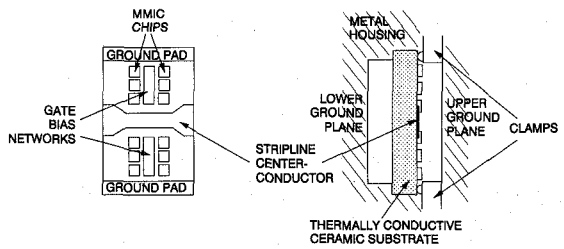

Fig. 6. Simplified drawing of the suspended stripline layout of the stack-FET switch elements. This hybrid circuit also includes the series capacitor, and the Z1 and Z2 line elements associated with each of the switches.

The physical line widths and propagation constants of the suspended striplines, including sidewall effects, were determined using a 2-dimensional finite element analysis program based on a simple relaxation algorithm for the static field solution. Measurements on a 50 Ω line section indicated that its characteristic impedance was accurate to within 4%.

In order to obtain acceptable yield, the total FET periphery required for each stack-FET switch element was divided into twelve MMIC chips, with five stacked FETs per chip. Two different FET topologies were used: the one shown in Fig. 4 has a conventional interdigitated structure and was used for the *S*-band switch. The Fig. 5 chip, used in the *C*-band unit, had a meandered gate configuration which minimized the number of air-bridges required. This allowed the FET length to be reduced to minimize parasitic inductance of the stack, while maintaining high chip yield. The Fig. 5 chip also included some compensation capacitors to overcome the parasitic capacitances between the stacked FETs and ground [4], and parasitics between FETs were reduced by omitting backside metallization of the chips.

We used a suspended-stripline hybrid circuit configuration to minimize loss and parasitic capacitances between the switch elements and ground. Although a microstrip format with multiple-gate FETs [2], [3] might have achieved similar results as far as the parasitics between the FETs and ground are concerned, the bias network parasitics would have been unacceptably high. Fig. 6 illustrates how the twelve MMIC stack FET chips for each shunt switch node are all mounted on one side of an aluminum nitride (AlN) substrate. This high thermal-conductivity ceramic was chosen over beryllium oxide to avoid the complications associated with handling toxic materials. A thin-film rf stripline center-conductor was deposited onto the same substrate. The symmetric layout of the MMIC chips on either side of the rf center-conductor minimized the parasitic series inductance of the shunt switch elements. For the *S*-band switch, the gate bias networks were fabricated on the AlN substrate as well, whereas for the *C*-band unit the bias network was fabricated on GaAs MMICs, which were then mounted next to the MMIC stack FET chips. Bond-wires were used to interconnect all components. The AlN substrate was suspended between two equi-distant ground planes, with the ambient air as a dielectric, and held in place using spring-loaded mounting clamps, which also provided the ground connection to the bottom of the FET stacks. This configuration allowed easy replacement of the switch elements and provided reliable thermal and electrical contact characteristics together with the necessary mechanical stress relief. The gate bias network was fed by a line (not shown

in Fig. 6) which passed underneath the mounting clamp and was connected to the driver circuit via a feedthrough mounted in a cavity beneath the lower ground plane.

IV. Driver Circuit Design

Fig. 7 shows a schematic diagram of the driver circuit used for the SPDT switches, based on a CMOS complementary-output driver chip. The passive components on the output of the driver chip generated about 15 ns differential delay between the positive and negative edges of the stack FET gate control line voltage transitions, so as to implement a make-before-break switching action. This means that, during a brief period, rf power was fed to both output loads simultaneously. As a result, the rf voltage swing seen by the FET stacks in each arm is decreased, thus minimizing the stress on the switch elements during the switching transients. Additional components were connected to the supply and TTL input lines for rf decoupling, and for supply polarity-reversal, overvoltage and latchup protection. The total quiescent power dissipation of the driver circuit was about 0.6 W, rising to 1.3 W at 1 MHz switching rate.

V. Assembly and Test

Epoxy was used to mount most of the components for each switch element of the AlN substrates. In the *S*-band switch, the stack-FET MMICs with highest power dissipation (in the elements closest to the input port) were soldered onto the substrate. We then tested the small- and large-signal performances of each switch element individually. For this screening procedure, we only had access to a medium-power TWT amplifier (6–10 W), which was hardly enough to adequately test the power handling capability of the elements in a 50 Ω system. However, by using a test fixture equipped with a narrow-band impedance transformation circuit, consisting of the C1, L1 and C2 elements in Fig. 8, we were able to apply an rf voltage swing equivalent to 125 W–200 W (in a 50 Ω system) to the stack FET elements in their 'off' state. The switch elements were then inserted into the SPDT switch unit housing, and no tuning adjustments were performed after assembly. Fig. 9 shows a picture of the *S*-band switch unit with the top ground-plane cover removed.

VI. Measured Performance

The results of a pulsed-rf test on a single shunt *S*-band switch element, in a 50 Ω system, are shown in Figure 10. Note that the element withstood pulsed input powers as high as 500 W, though its insertion loss increased substantially at input levels beyond 300 W. Based on previous measurements made on switches fabricated with smaller FET stacks [4], but similar FET characteristics, we expected the insertion loss to remain fairly constant up to about 400 W. It is probable that the rf voltage distribution within the FET stack was not as uniform as expected, leading to a less-well defined compression point.

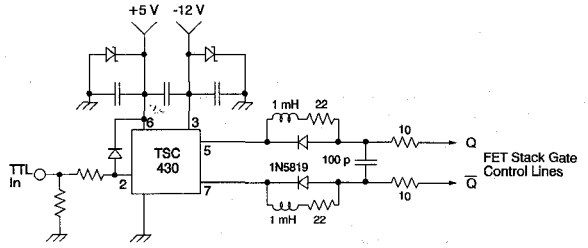

Fig. 7. Driver circuit schematic.

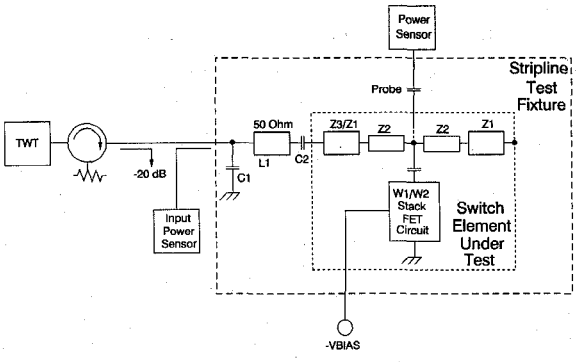

Fig. 8. Test circuit used for large-signal screening of the switch elements. A probe protruding through the top ground-plane of the fixture was used to measure the rf voltage swing across the FET stack.

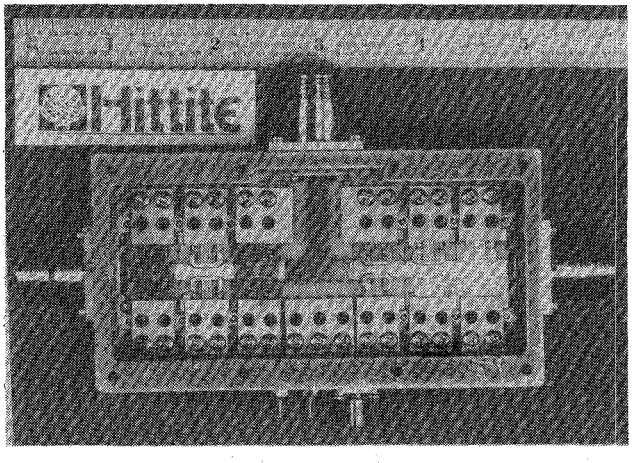

Fig. 9. Picture of the *S*-band switch unit.

Fig. 11 shows the measured small-signal insertion loss and isolation vs. frequency for one arm of the fully assembled *S*-band SPDT switch unit shown in Fig. 9. The return losses of the common and output ports of the same switch are plotted in Fig. 12. The *C*-band unit had a minimum small-signal insertion loss of 1.55 dB at 5.4 GHz and an isolation better than 40 dB over a 10% bandwidth. Fig. 13 shows oscilloscope traces of the rf power output from both arms of the *S*-band switch during the switching transient; 10–90% rf amplitude rise-fall times of less than 40 ns were obtained from both units. The intermediate steps in the Fig. 13 traces are due to the make-before-break delay built into the switch driver. Figs. 14 and 15 show the measured insertion loss and isolation of the *S*-band unit versus the CW input power level, respec-

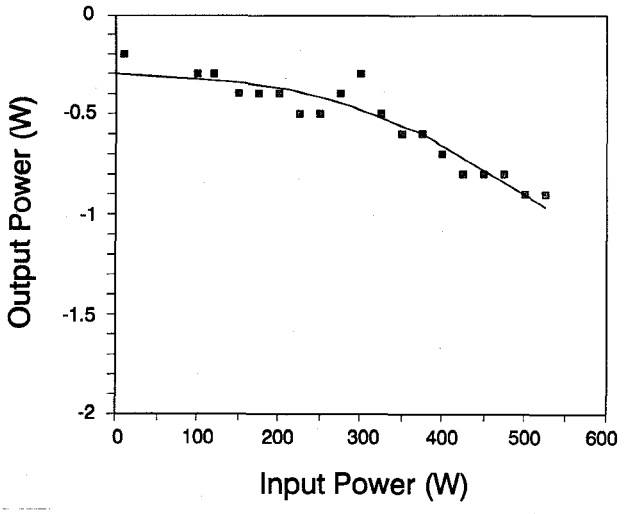

Fig. 10. Measured insertion loss of a single shunt switch element versus pulsed-rf input power (1 μs pulses, F_{rf} = 3.4 GHz).

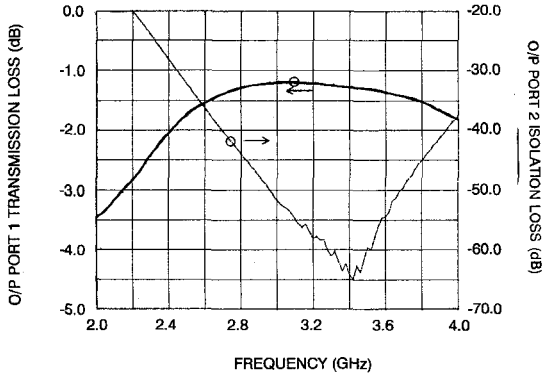

Fig. 11. Measured small-signal insertion loss and isolation frequency responses of the *S*-band switch unit.

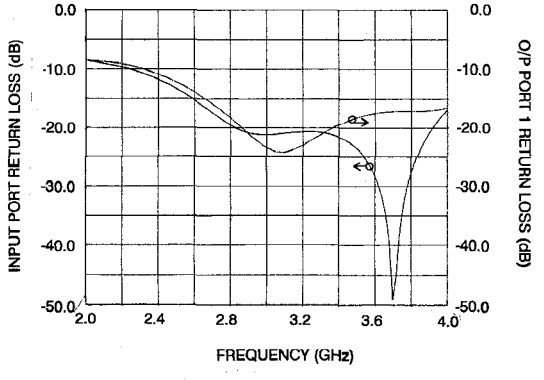

Fig. 12. Measured small-signal return losses at the rf input and output port of the *S*-band switch unit.

tively. A sustained hot-switching CW input power handling capability of 300 W was demonstrated with this unit, up to a switching rate of 500 KHz (the highest switching signal frequency we applied during power tests). Fig. 16 is a plot of output power versus input power for the *C*-band switch, under pulsed rf conditions, showing that no significant compression was observed up to about 200 W input power level. Fig. 17 is a plot of output versus

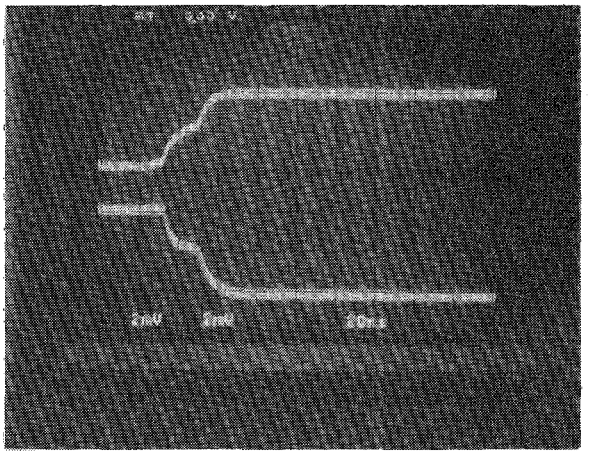

Fig. 13. Oscilloscope traces of the output power from both arms of the *S*-band switch unit during switching transients (H. axis = 20 ns/div, V. axis = 1 W/div).

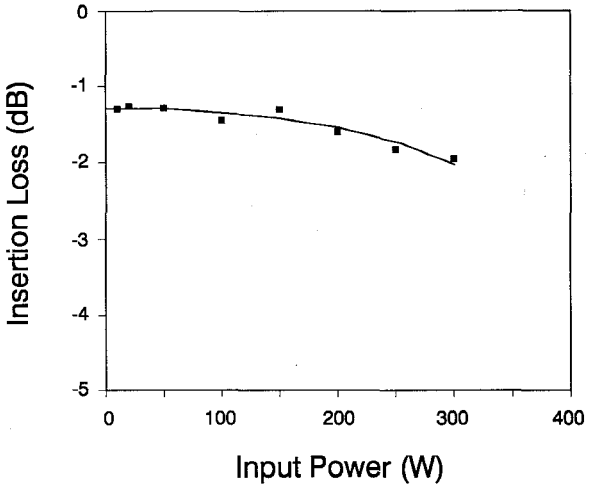

Fig. 14. Measured insertion loss vs. CW input power for the *S*-band switch unit (f = 3.3 GHz).

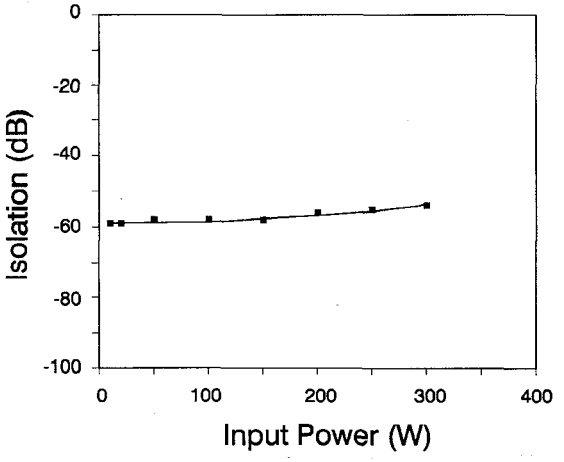

Fig. 15. Measured isolation versus CW input power for the *S*-band switch unit (f = 3.3 GHz).

CW input power for the *C*-band switch unit under hot-switching conditions. The CW power handling capability of this switch was not as high as the *S*-band one, due to

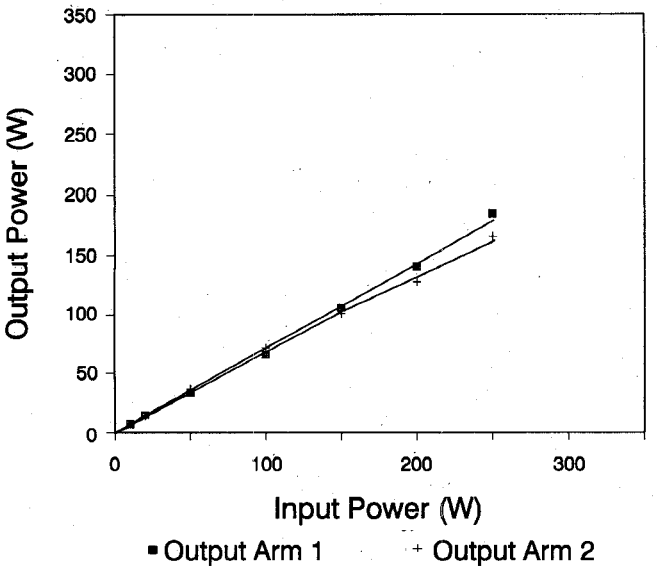

Fig. 16. Measured output power versus pulsed-rf input power for the *C*-band switch unit (f = 5.6 GHz, 10 μs pulses).

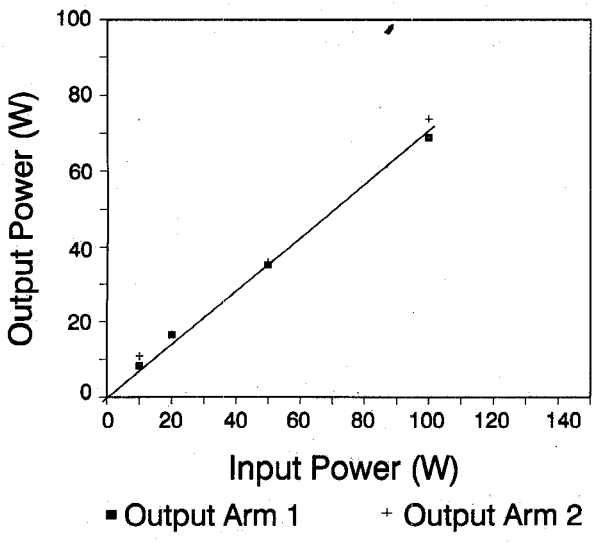

Fig. 17. Measured output power versus CW input power for the *C*-band switch unit, under hot-switching conditions (f = 5.6 GHz, 100 kHz switching rate).

voids in the thermally conductive epoxy layer bonding the MMIC chips to the AlN substrates.

VII. Conclusion

We have demonstrated that GaAs, MESFET-based MMIC technology is a viable option for the design of high-power microwave switches in the 100+ watt range, and it is especially attractive in applications which require fast transitions, or hot-switching at high switching rates. Further work should concentrate on reliability aspects of this technology and on improving insertion loss, bandwidth, and power handling characteristics, possibly through use of multiple-gate and/or insulated-gate devices, and more accurate modeling of the circuit parasitics.

Acknowledgment

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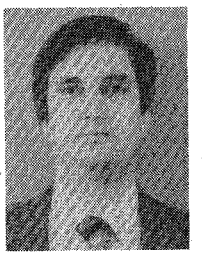
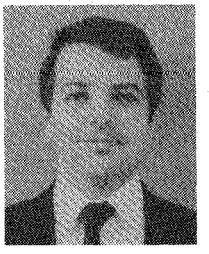


Peter Katzin (S'82–M'82) received the B.S. degree in Physics and Electrical Engineering from the University of Manchester, England, in 1979. His graduate study was at Cornell University, where he received the M. Eng. degree in Electrical Engineering in 1983.

From 1980 to 1981, he was with the Space and Communications Division, Hughes Aircraft Company, where he contributed to the design and testing of the attitude control and the microwave command, tracking, and ranging systems of communication satellites. In 1983, he joined the research division of Raytheon Company. There he was responsible for the evaluation and development of GaAs MMIC components and circuits, including 44 GHz power amplifiers and high-efficiency switching power amplifiers.

In 1987, he joined the Hittite Microwave Corporation where he has been responsible for development of MMIC approaches to high-power switches, broadband circulators, GPS frequency translators, and filters. He is also involved in the design of MMIC-based FM-CW radar ranging systems.

Mr. Katzin is the author/co-author of several technical papers.



Brian E. Bedard received the B.S. degree in electrical engineering from the University of Lowell in 1976, graduating Summa Cum Laude. He later received his M.B.A. degree from Northeastern University in 1984.

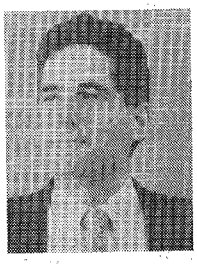
In 1976, he joined Motorola, Inc., Communications Division, where he engaged in receiver design of radio paging products. He was awarded two patents related to a 900 MHz stripline bandpass filter.

In 1979, he joined Sanders Associates, Micro-

wave Division, where he participated in Phase I of the ASPJ Program as part of the Advanced Development Group.

In 1981, he moved on to Adams-Russell, where he participated in the start-up of the Gallium-Arsenide Semiconductor Center as the Product Engineering Manager responsible for all GaAs MMIC circuit design. In this capacity, he directly designed several switch MMICs and an L-band VCO/buffer MMIC, in addition to supervising the design of several MMIC amplifiers. In 1986, he managed the design of a control device product line based on GaAs technology which has enjoyed significant success in the marketplace.

In 1988, Mr. Bedard joined Hittite Microwave Corporation where he is currently engaged in the design of novel MMIC products.



Mitchell B. Shifrin (M'86) received two B.S. degrees from the University of Wisconsin, Madison in 1980: one in electrical and computer engineering, and the other in applied mathematics and engineering physics. In 1980, he received a Raytheon Company Fellowship which enabled him to attend the University of Massachusetts, where in 1981 he received an M.S. degree in electrical engineering. He concentrated his studies in the areas of solid-state devices and microwave circuits.

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Dr. Ayasli has been involved in theoretical and experimental studies of Microwave Monolithic Integrated Circuit techniques involving GaAs Field-Effect Transistors (FETs) and related devices since 1979. He managed research and development programs at Raytheon Research Division which included circuit design, semiconductor wafer processing, and device measurement and characterization. In this capacity, he was the program manager for several government R&D programs for wide-band amplifiers and Transmit/Receive modules.

In addition, he is the author of a number of technical papers and holds several patents related to FETs and their monolithic applications. He was the General Chairman for the 1987 IEEE Microwave and Millimeter Wave Monolithic Circuits Symposium. He is also co-recipient of 1986 IEEE Microwave Prize for his work on wide-band monolithic traveling wave amplifiers.